AMENDMENTS TO THE CLAIMS:

1. (ORIGINAL) A method of controlling a flow of serial data across an Radio Frequency (RF) barrier of an RF enclosure, comprising:

a processor sending one or more control data using one or more lines of a serial control data bus;

an interface electronics module, receiving the one or more lines of the serial control data bus and selecting one or more signals corresponding to one or more addresses of the one or more lines; and

the interface electronics module, sending the selected one or more signals to an electronics module within the RF enclosure.

2. (ORIGINAL) The method of claim 1, wherein selecting the one or more signals further comprises selecting each signal with a same line value.

3. (ORIGINAL) The method of claim 1, wherein the processor is a microprocessor.

4. (CURRENTLY AMENDED) The method of claim 1, wherein integrated circuit technology is ~~techniques are~~ used to select the one or more signals.

5. (ORIGINAL) The method of claim 1, wherein the serial control data bus is an SPI bus.

6. (ORIGINAL) The method of claim 1, wherein the one or more signals are selected by the processor.

7. (ORIGINAL) The method of claim 1, wherein the interface electronics module further comprises an RF filtered connector.

8. (ORIGINAL) The method of claim 7, wherein one or more Schmitt trigger input buffers are used to eliminate potential noise problems caused by the RF filtered connectors.

9. (ORIGINAL) A structure for controlling a flow of serial data across an Radio Frequency (RF) barrier of an RF enclosure, comprising:

a processor, operable to send and receive data, coupled to one or more lines of a serial control data bus;

an interface electronics module, operable to select one or more signals corresponding to one or more addresses of the one or more lines of the serial control data bus, said RF interface module coupled to an RF enclosure; and

an electronics module physically located within the RF cavity, operable to receive the one or more lines selected by the interface electronics module, said electronics module coupled to the interface electronics module.

10. (ORIGINAL) The structure of claim 9, wherein the interface electronics module selects each signal with a same line number.

11. (ORIGINAL) The structure of claim 9, wherein the processor is a microprocessor.

12. (CURRENTLY AMENDED) The structure of claim 9, wherein integrated circuit technology is ~~techniques are~~ used to select the one or more signals.

13. (ORIGINAL) The structure of claim 9, wherein the serial control data bus is an SPI bus.

14. (ORIGINAL) The structure of claim 9, wherein the one or more signals are selected by the processor.

15. (ORIGINAL) The structure of claim 9, wherein an RF filtered connector is coupled to the interface electronics module and to the RF enclosure, said RF enclosure providing an interface to the RF cavity.

16. (ORIGINAL) The structure of claim 15, wherein one or more Schmitt trigger input buffers are used to eliminate potential noise problems caused by the RF filtered connectors.

17. (ORIGINAL) The method of claim 1, wherein sending the selected one or more signals to the electronics module within the RF enclosure is performed in accordance with a gating functionality of the interface electronics module.

18. (ORIGINAL) The method of claim 17, wherein the gating functionality is a temporal gating functionality.